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SAN FRANCISCO, CA, USA

Chiplet and Die-to-Die (D2D) Interface Interoperability How to Accelerate the Path to an Open Ecosystem

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Alphawave Semi

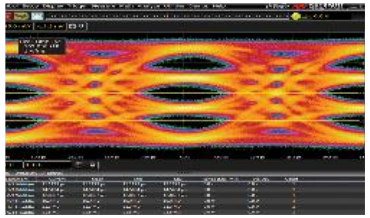
Outline

- Introduction
- Chiplet-Based Design Motivations
- Technology Enablers
- Open Ecosystem Key Enablers
- Usage Models and Building Blocks
- Decision Matrix
- Conclusion

Alphawave Semi Technology Strengths

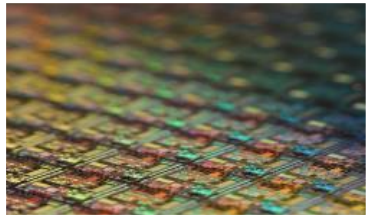
Leading Edge Capabilities and Technologies to Deliver the Fastest Connectivity Solutions

High-Speed Connectivity IP



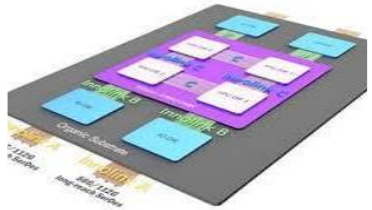
- 224Gbps,112Gbps, chiplets
- #1 TSMC OIP partner 2020-2022
- 2022 Samsung Best Collaboration Award

Advanced Silicon



- First in 7nm, 6nm, 5nm, 4nm, and 3nm

Chiplet – Package Design



- Deep expertise in chiplet package design
- 2.5D and 3D package designs in production

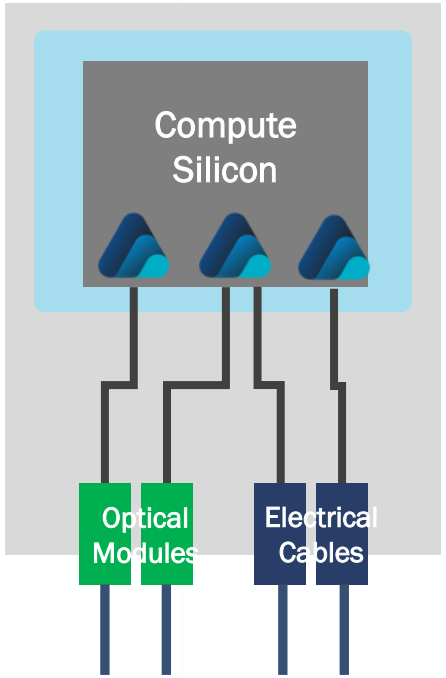
Opto-Electronics

- PAM4, Coherent DSPs, and silicon photonics for 1.6T Ethernet
- 224Gbps photonics in silicon

Delivering Optimized Data Infrastructure Solutions - Faster

The Evolution of Data Center Silicon: A Growing Opportunity For Chiplets

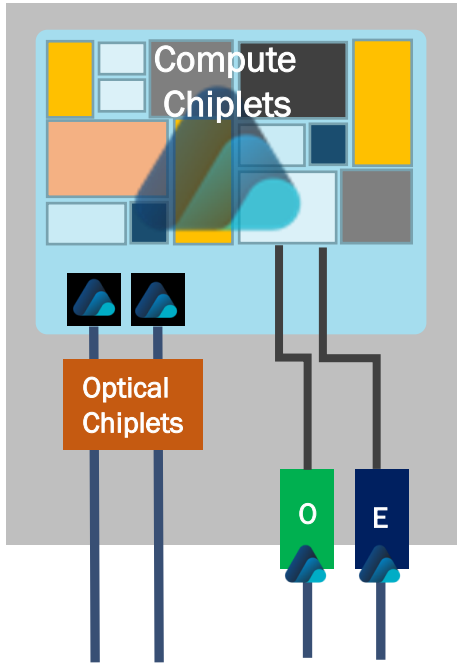
N-1 Silicon Designs



Technology 16/12/7nm

- >$250M cost of design
- >2 years design cycle
- Silicon costs increasing in advanced technologies

N+1 Silicon Designs



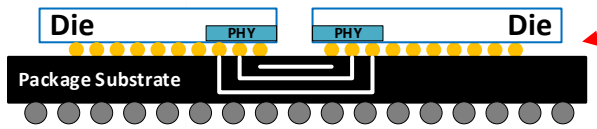
Technology 7/5/3nm

- Use prebuilt chiplets
- Higher bandwidth and lower power
- Cost-effective, flexible approach

- Accelerate the rollout of AI/ML at scale for more system functionality at a cost-effective price (up to 35%)
- Lower overall system power while increasing throughput (up to 30%)
- Reduce risk and time-to-market by reusing silicon-proven IPs and older technologies
- Unleash creation of new product variants for flexible portfolio management

Package Technology Enablers

Standard Package
C4 bump 110-130um pitch
High Yield
$

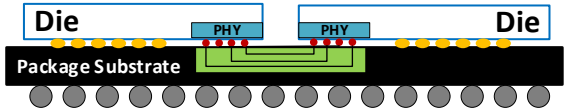


Organic Substrate

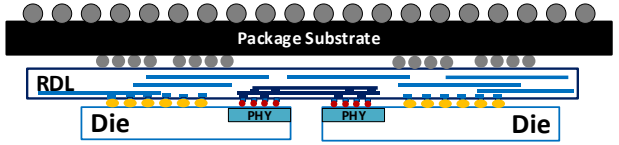
C4

Advanced Package
C4 bump 110-130um pitch
uBump 45-55um pitch
High-Moderate Yield
$$

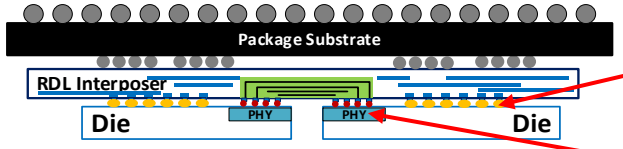
Embedded Bridge



Integrated Fan Out RDL



Integrated Fan Out LSI

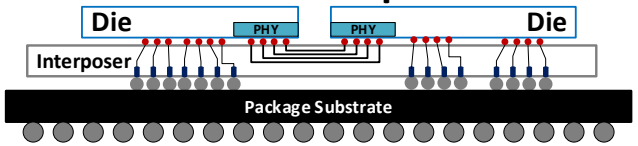


C4

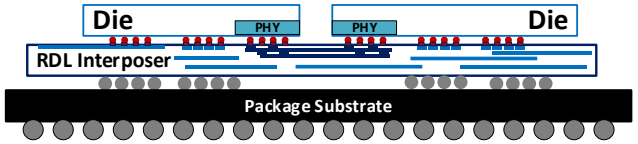
uBump

Advanced Package
uBump 45-55um pitch
Moderate-Low Yield
$$$

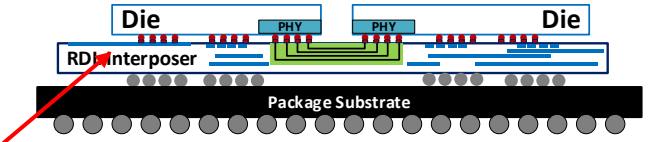
Silicon Interposer



CoWoS-R



CoWoS-L



Chiplets Enabled by High-Speed Die-to-Die (Data) Links

Alphawave Semi is at the Forefront of the New Chiplet Design Paradigm

Bandwidth Density — Linear & Area

Throughput achievable over a single link: data/time

The higher the better

Power Consumption — Energy Efficiency (pJ/b)

Main operating cost / Impact of heat dissipation on reliability

Low-power modes and flexible power supplies

Latency — End-to-end: Tx+Rx

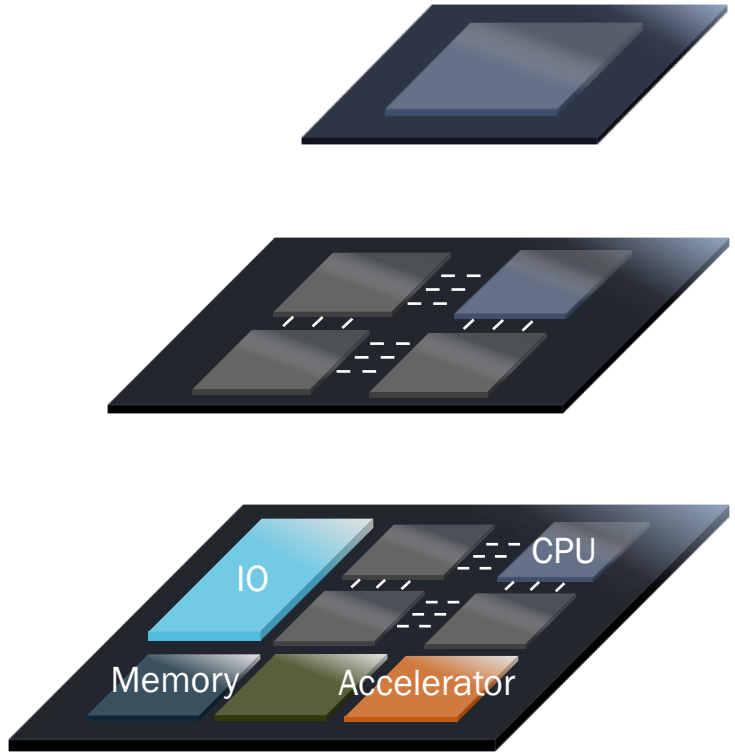
End-to-end travel time for data

Require dedicated solutions for applications where (low) latency is critical

Robustness — Reliability & BER

Work reliability of the link in every environment

Highly reliable, reconfigurable, and adaptive



D2D Interface Standardization Efforts

UCIe Universal Chiplet Interconnect Express

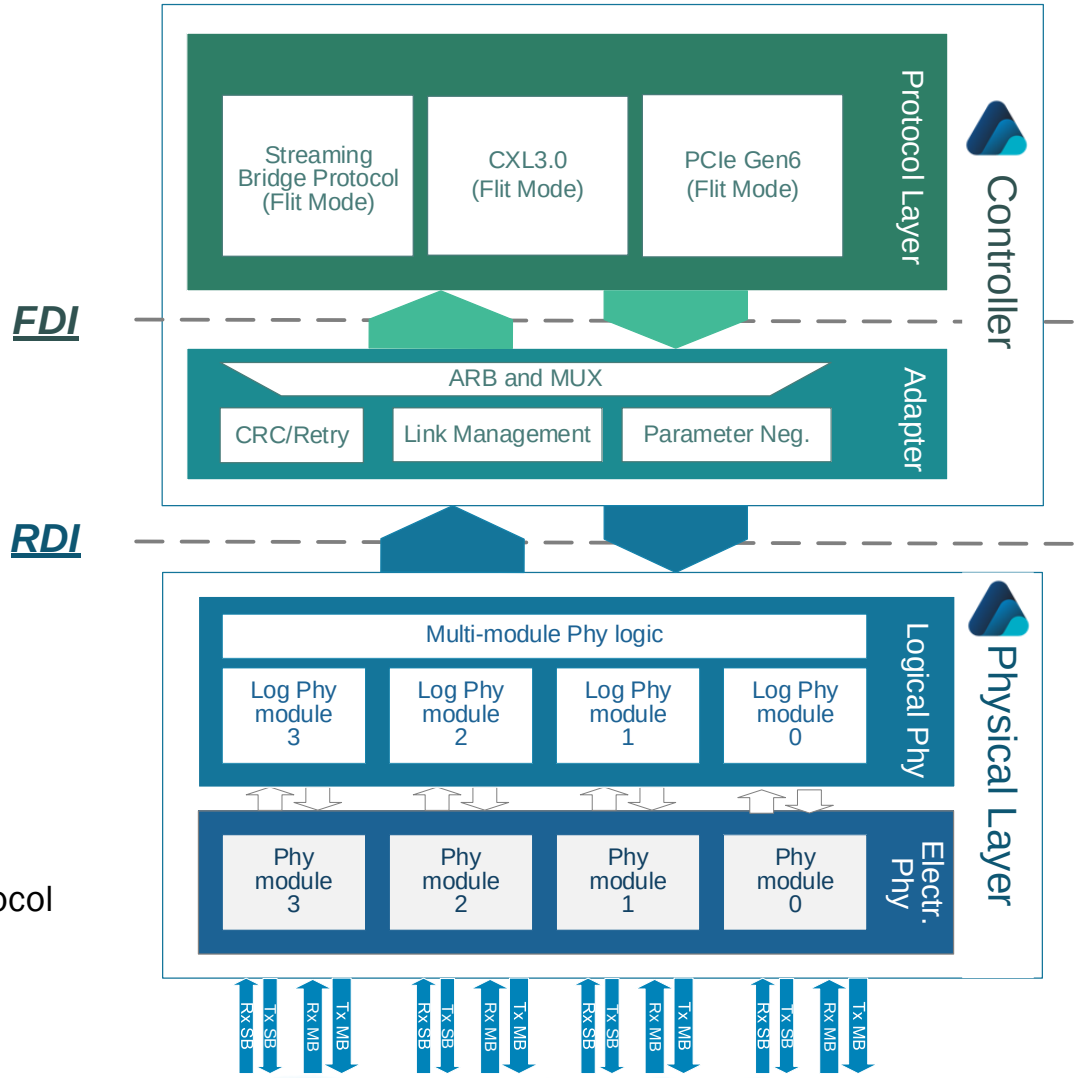
OPEN Compute Project®
Open-Domain-Specific-Architecture

Parameter	Advanced Package		Standard Package		
	OpenHBI 1.0/2.0	UCIe- Advanced	BOW FAST	OpenHBI-L	UCIe -Standard
Data Rate [Gbps]	8/16	4/8/16/**24/32**	16	40	4/8/16/**24/32**
IO Swing [V]	0.4	0.4/0.7	0.75	0.75	0.4/0.7
(Tx+Rx) Data/Channel	40	64	32	40	32, 16,
Edge Density [Tbps/mm]	4.2	4.2 (16G)	0.9	1	0.9 (16G, x16) 1.8 (16G, x32)
Reliability (BER)	1e-25	1e-25	1e-15	1e-15	1e-15
(Tx+Rx) PHY Latency	~2ns	~2ns	~2ns	~4ns	~2ns
Power Efficiency (pJ/b)	<0.35	0.3 <16G 0.5 >16G	0.5	0.5	0.5 <16G 1.0 >16G
Bump-Out/FormFactor	Specified	Specified	Partially	Specified	Specified
Logical PHY/Interface	Specified	Specified/RDI	Roadmap	Specified	Specified/RDI
Protocol Layer	Not Specified	Streaming/ PCIe/CXL	Not Specified	Not Specified	Streaming/ PCIe/CXL
Compliance Platform	Not Specified	Roadmap	Not Specified	Not Specified	Roadmap

- D2D Interface Standardization is the most important step in introducing a Chiplet Ecosystem
- UCIe offers complete specifications meeting all key performance attributes:
  - Physical
  - Protocol
  - Platform Compliance

Alphawave Semi UCIe Complete Solution for an Open Ecosystem

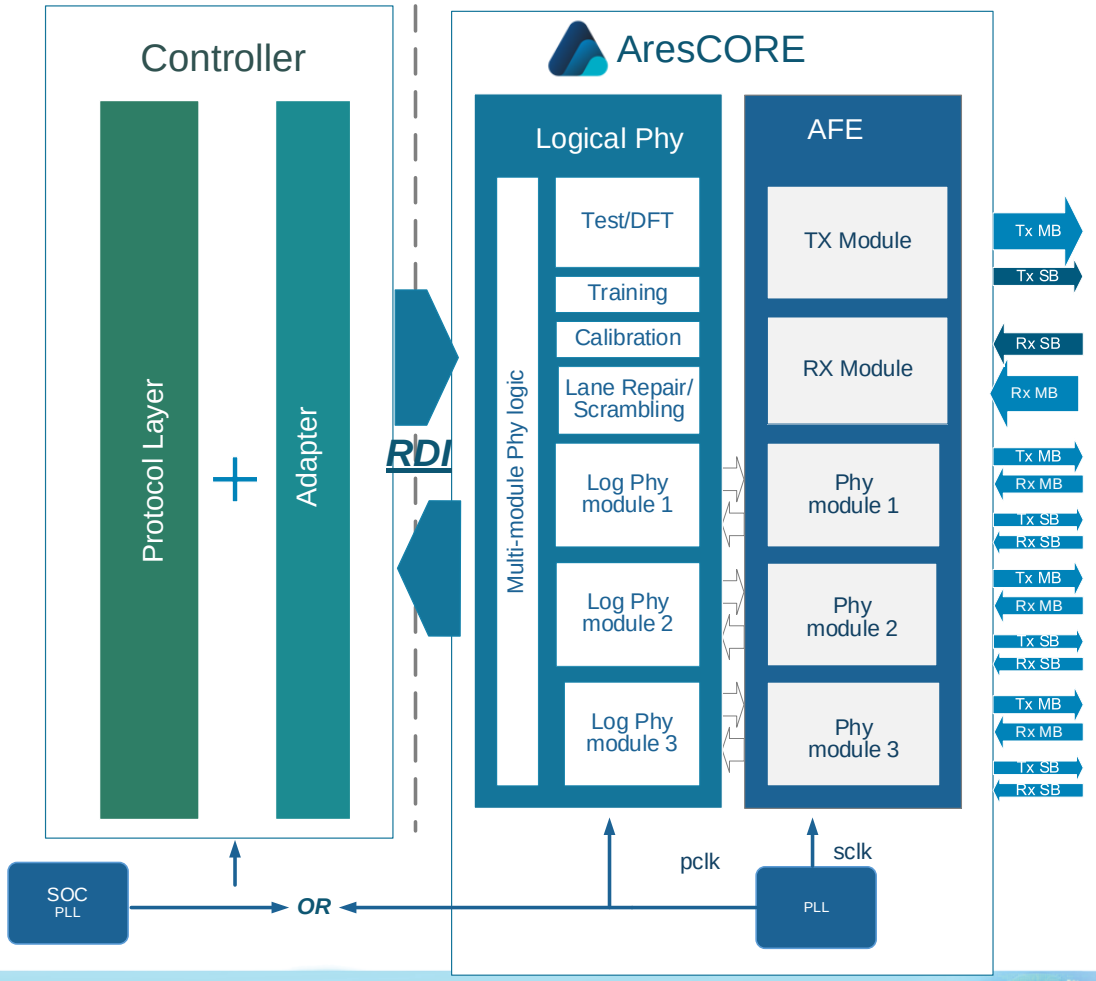
- **UCIe Physical Layer**
  - Electrical PHY (AFE) leveraging silicon-proven analog IP
  - Includes clocking, link training, sideband signals
  - Logical PHY including Multi-Module PHY logic
  - Top-level floorplan for all flexible package options
- **UCIe Die-to-Die Adapter**
  - Provides link state management
  - Parameter negotiations key for chiplet interop
  - Manages reliable link implementing CRC and link level retry
- **Protocol Layer**
  - Maps PCIe and CXL protocol natively via Flit-Aware Mode
  - Also provides Streaming Protocol Bridge, enabling different type of SoC interfaces
- **Form Factor and Interoperability**
  - Alphawave provides a platform for electrical, physical form factor, and protocol compliance
  - Complete set of test vehicles for interoperability testing



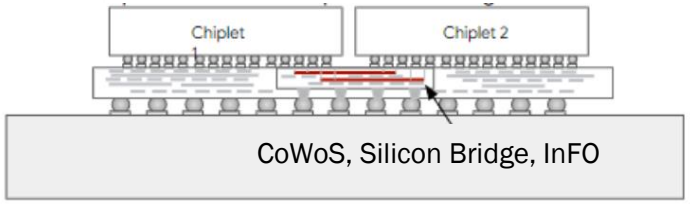
Alphawave Semi UCIe PHY Solutions

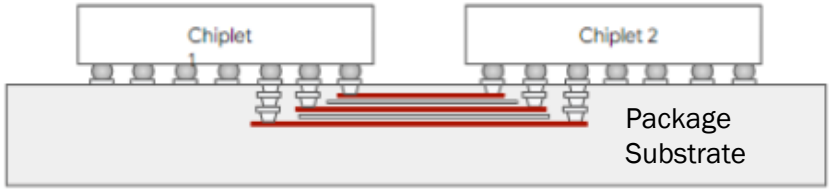
AresCORE – Low Latency, High Throughput and Reliable Die-to-Die Interface

- The AresCORE D2D PHY can be configured to be compliant with:
  - UCIe Standard MODULEs of 16bit and 32bit
  - UCIe Advanced MODULEs of 64bit
  - Leveraging silicon-proven analog IP blocks available in advanced technology nodes (7nm, 5nm, 3nm)
- Optimized for High-Bandwidth density, Low-Power, Low-Latency multi module PHY
  - Up to 24Gbps per data pin
  - Low Latency Tx+Rx datapath
  - Low Power Energy per wire
  - Optimized BW/mm2 for both Advanced and Standard Packages
- Delivered as Fully-Integrated Solutions
  - Equipped with full Calibrations, Training, DFT, and Reliability features
  - Optimized for E/W and N/S implementations
  - Delivered as subsystem to support RDI or pre-integrated with Streaming or PCIe/CXL Controller



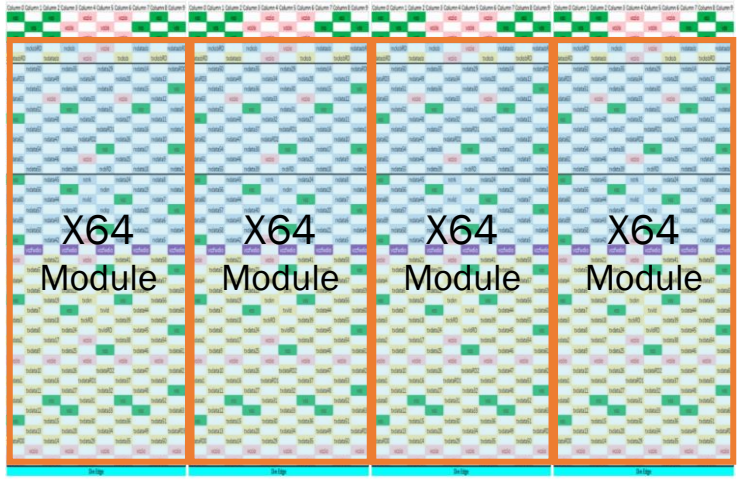
AresCORE UCIe PHY Support for All Package Types





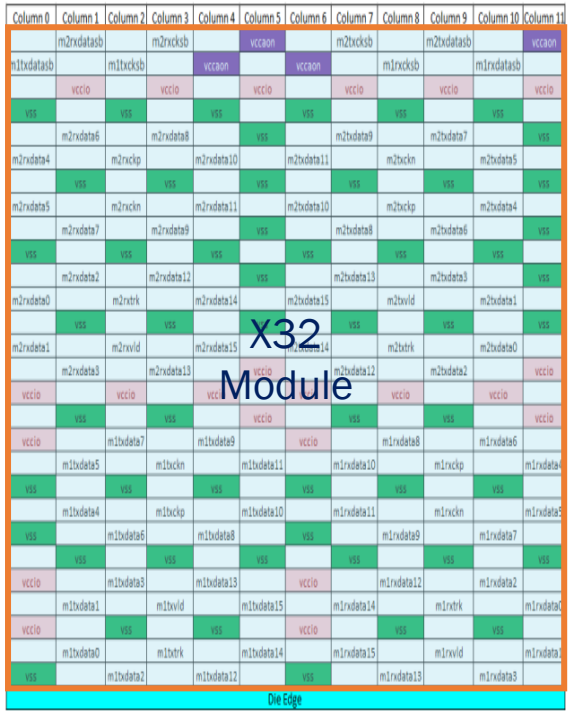
Advanced Package

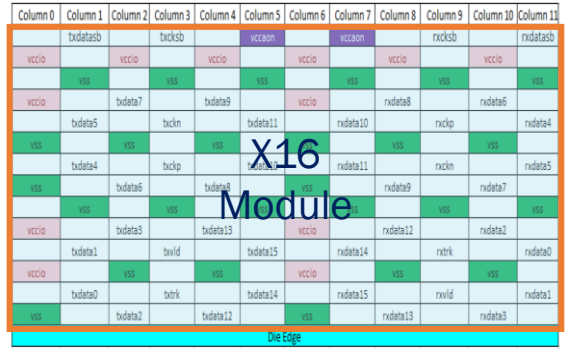
- 2Tbps per Module @16Gbps
- 45um bump pitch
- 64Tx+ 64Rx per Module
- 1 / 2 / 4 Module Configuration Support
- Shareable PLL



Standard Package

- 1.5 or 0.77Tbps per Module @24Gbps
- 110um bump pitch
- 16Tx+16 Rx
- 1 / 2 / 4 Modules
- Shareable PLL

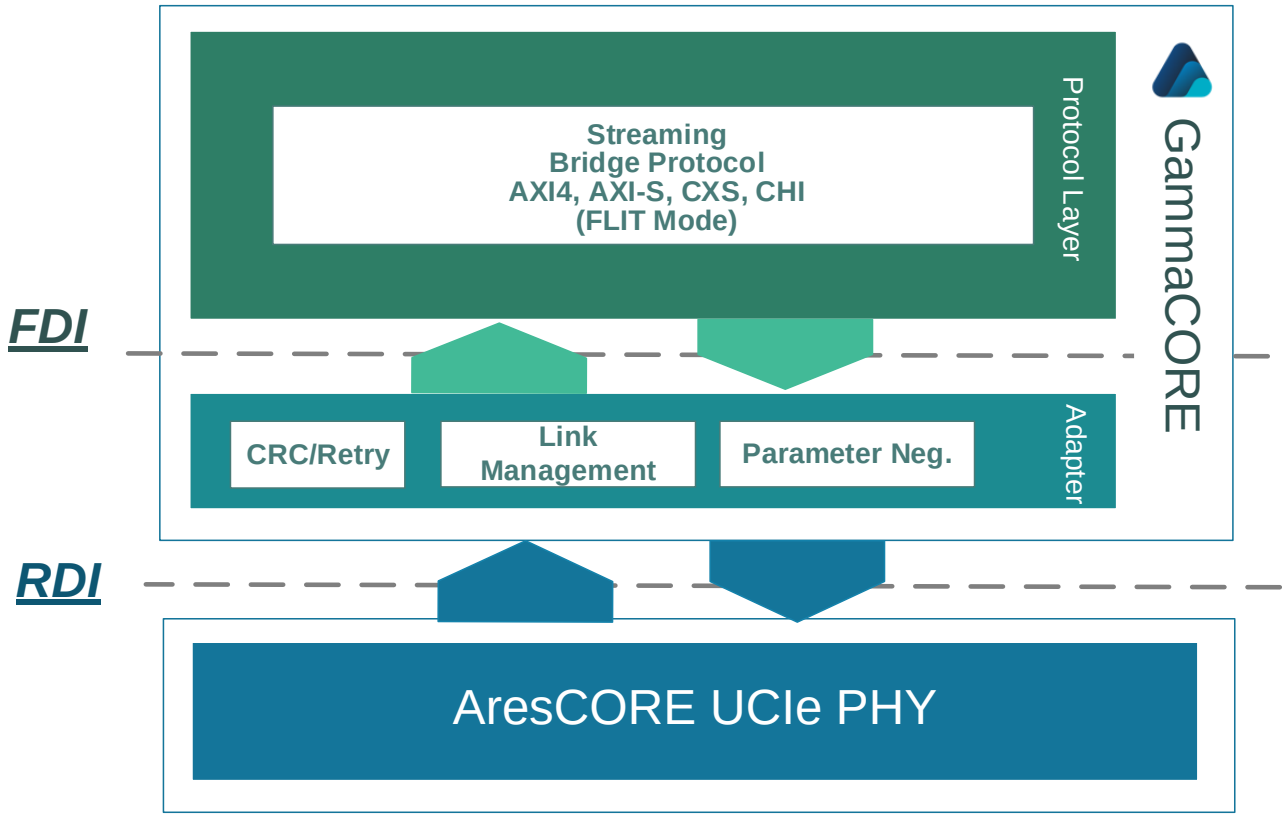




Alphawave Semi Streaming Protocol and Adapter

GammaCORE - Low Latency and Flexible Streaming Protocol for Adaptations of NoC SOC Interfaces

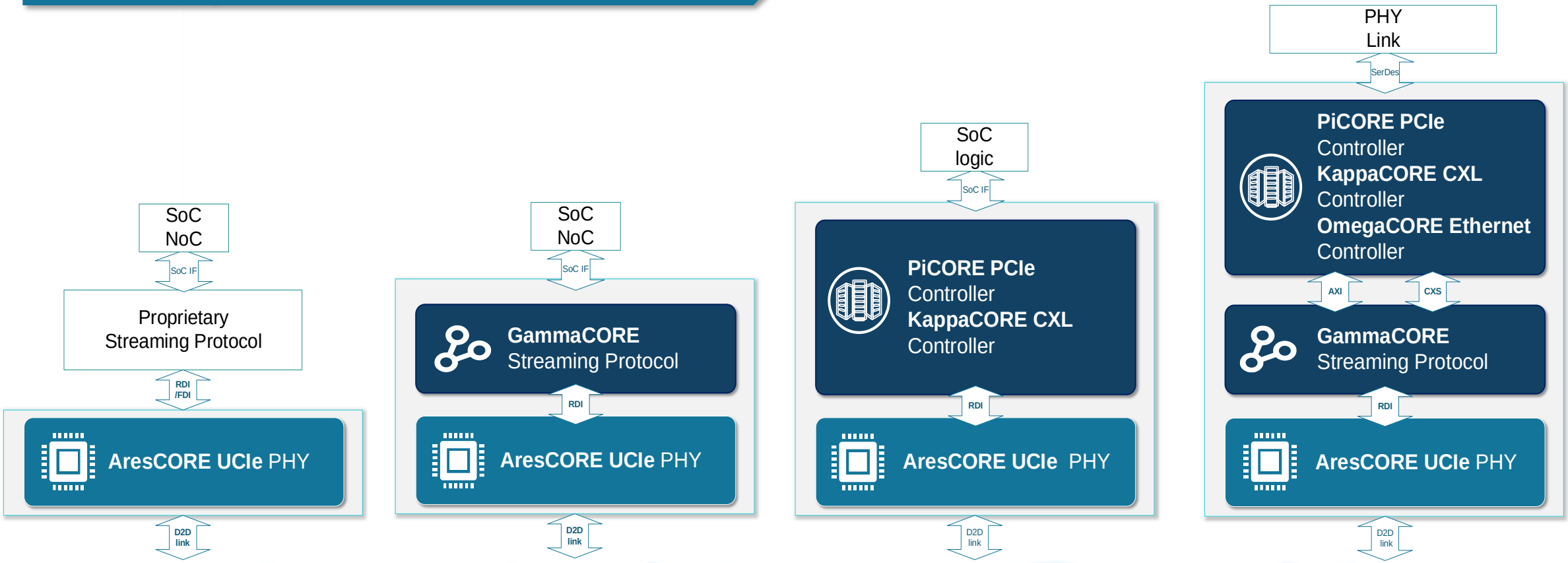
- Supports UCIe's CRC/Retry and optional parity for runtime link test.
- Supports AXI4, AXI-S, CXS, CHI, or proprietary SoC I/Fs.
  - Any number of ports (single/multi-ported configs), any number of channels per port, any channel width.
  - Optional clock domain crossing between SoC and UCIe controller clocks.
- GammaCORE supports multiple datapath width options to address specific bandwidth and target clock frequency requirements.



Alphawave Semi UCIe Building Blocks

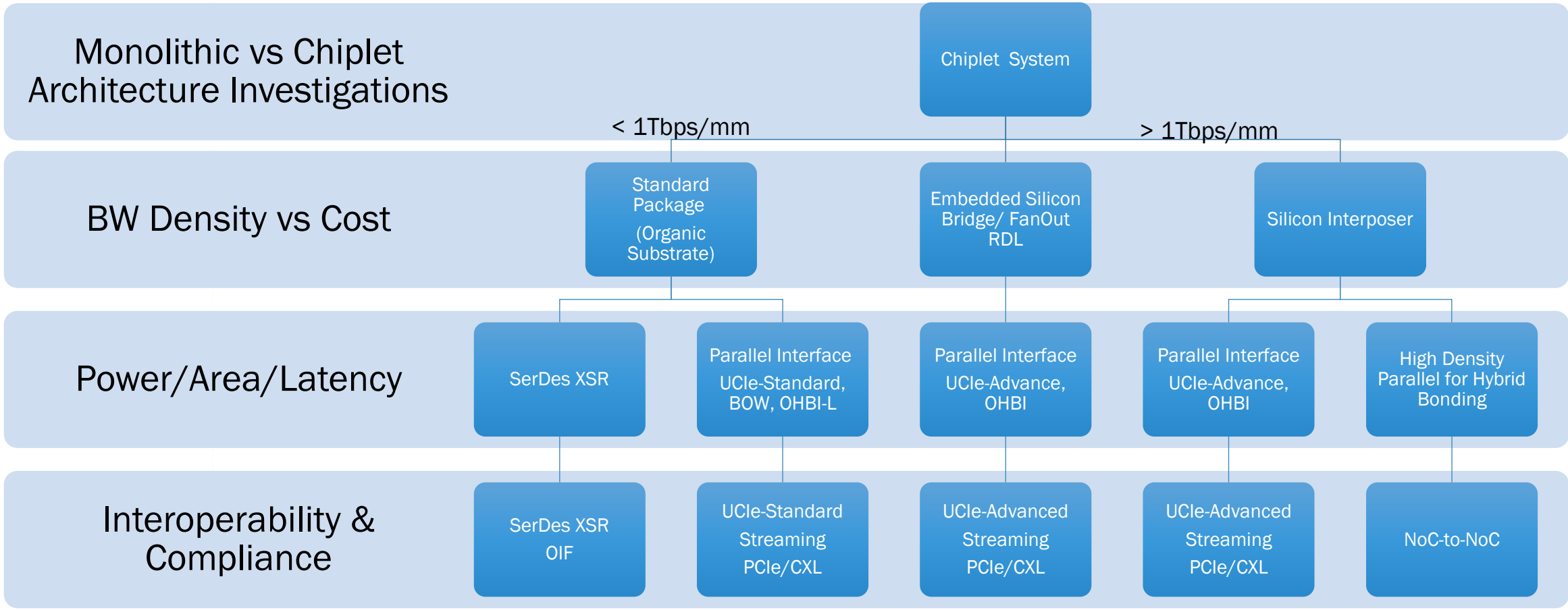
Low Latency | Coherency and Interoperability | Aggregation Interface

Low Latency User Defined Interface



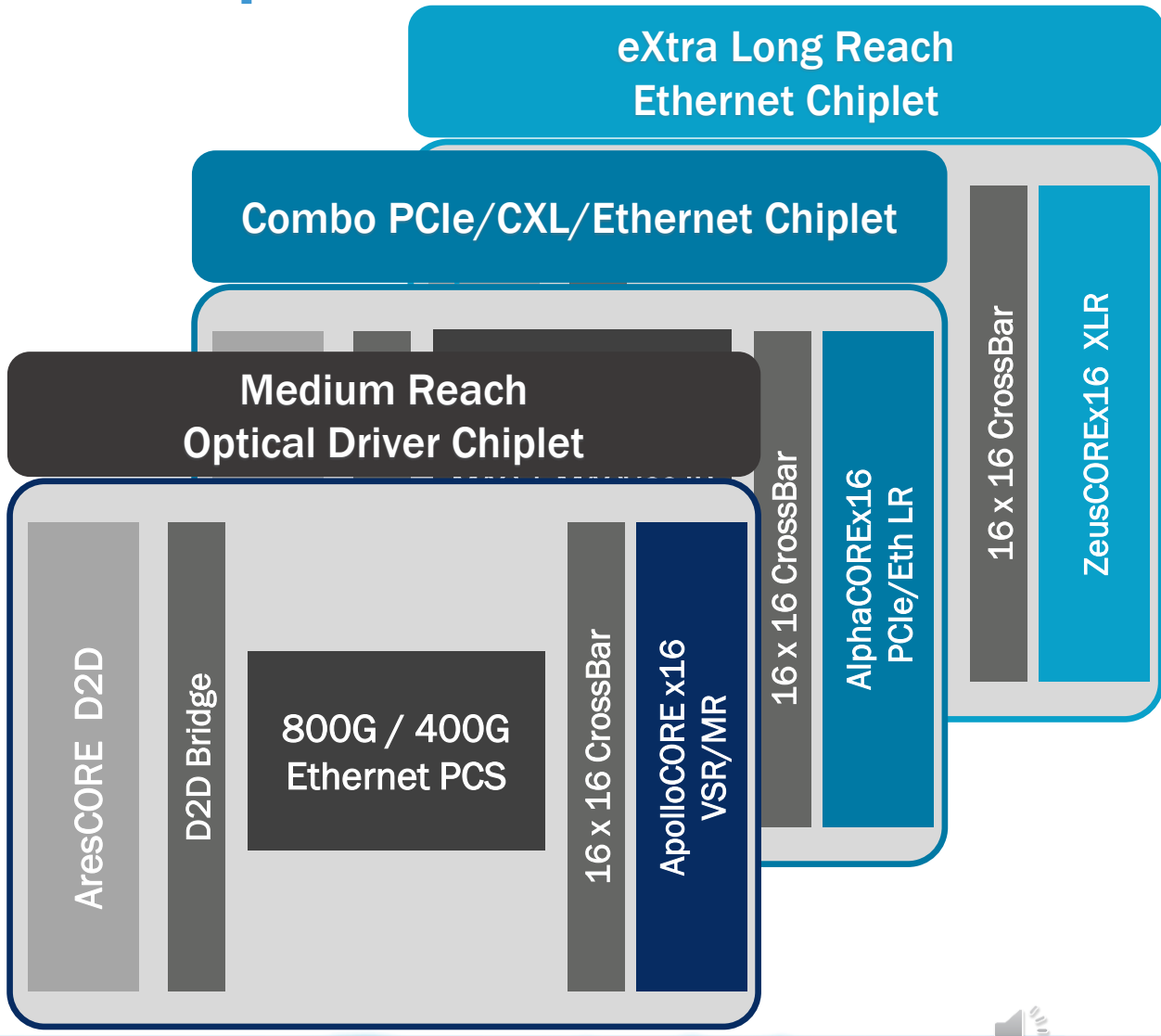
Decision Matrix for a Chiplet System

How to Navigate Today Chiplet Based Design



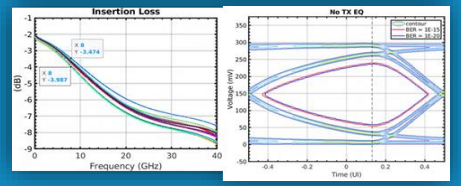
Open Ecosystem Drives Chiplets Adoption

- Leverage Alphawave Semi Connectivity IP and subsystems to accelerate Chiplet Adoption
- Alphawave Chiplets are customizable based on target applications
- Flexible engagement model for fast Time To Market (TTM)
- Delivered with full set of industry-standard collaterals
  - RTL to GDS
  - DFT and ATE testing
  - SI/PI and Thermal Models
  - FW/API Support
  - Product Lifecycle Management
- Alphawave Semi is committed to expanding the adoption of D2D connectivity and Chiplets into the Open Ecosystem

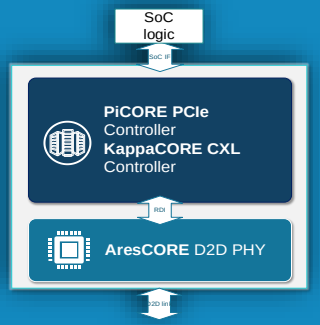


Beyond just IP: Alphawave Semi SoC Life Cycle Support

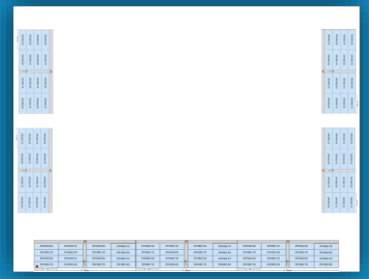
Leverage High Speed PHY Design Expertise and Silicon Proven IP Block



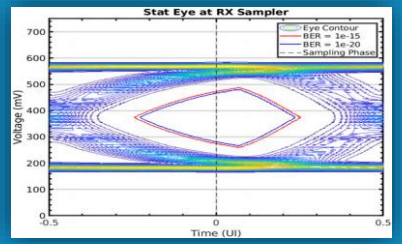
Complete D2D UCIe Verified IP SubSystem



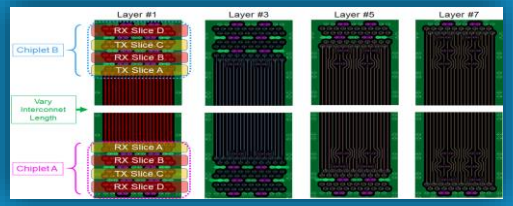
Expertise in Complex Physical Integration



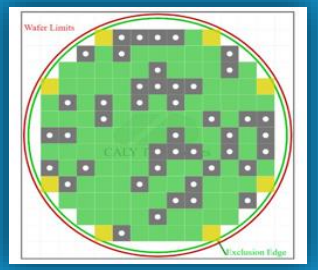
System Level Modelling Bit Level Accurate Model SI/PI for all Channel Types



Unparalleled expertise on Advanced Package Design for High-Speed Interfaces



Leverage Alphawave Chiplet and SoC Experience



Best PPA for a low risk and fast time-to-market D2D IP intercept

Conclusions

In more advanced manufacturing nodes, chiplets provide benefits across a broader range of SoC design compositions than legacy technologies

In today's application and system-driven world, it is extremely important to have Interface IPs and a Chiplet ecosystem that accelerates innovation

UCIe D2D Standard is the most important step toward an Open Ecosystem

Existing and new usage models are now possible with higher package-level integrations, delivering power-efficient and cost-effective performance

Alphawave Semi offers complete Die-to-Die IP Subsystem Solutions and Chiplet Architectures for the next generation of System-in-Packages